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| ART UNIT | PAPER NUMBER |
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| 2114 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/828,983 | RAPAICH, MARK | |
| | Examiner | Art Unit | |
| | Joseph Schell | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## *Detailed Action*

Claims 1-28 have been examined.

Claims 1-28 have been rejected.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 4 (line 2) and 12 (line 4) use the limitation of "activating a flash visual indicator." This limitation is not well known within the art and not clearly defined within the specification. In view of paragraph 16 of the specification, examiner is interpreting this limitation as a visual indication of a peripheral failure.

2. Claim 27 line 2 states the limitation "said computer system." This limitation lacks antecedent basis within the claim.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-7, 9-11, 13-15, 17-19, 21 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowan (US Patent 6,098,182) in view of Dai (US Patent Application Publication 2002/0032885).

4. As per claim 1, Cowan ('182) discloses an apparatus for detecting and indicating faults on a computer motherboard comprising:

a microprocessor capable of requesting and retrieving a plurality of diagnostic instructions (the remote PC as shown in Figure 5, and executing instructions, see column 1 lines 27-32);

a nonvolatile memory device having said plurality of diagnostic instructions stored (column 1 lines 27-32); and

a visual indicator coupled to said microprocessor indicating a fault on said computer motherboard (column 1 lines 35-43).

Testing by Cowan ('182) is performed within a TSR (column 4 lines 1-6). Cowan ('182) does not expressly disclose the apparatus comprising: said microprocessor executing said retrieved plurality of diagnostic instructions when said microprocessor receives an initialization signal, said plurality diagnostic instructions initializing said computer motherboard and a fault is indicated if said computer motherboard is not successfully initialized.

Dai ('885) discloses a BIOS test performed at power-on (paragraphs 7 and 9) that outputs test results to a series of LEDs (paragraph 14). BIOS performs initialization routines for a motherboard (paragraph 9, BIOS are the first program run) wherein an initialization signal that starts the BIOS is a power up signal.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the testing performed by Cowan ('182) such that testing is performed on power up by the BIOS, as taught by Dai ('885), instead of within a TSR as disclosed by Cowan ('182). This modification would have been obvious because problems should be found before starting other (application) operations to ensure that the computer is running in the optimal mode (Dai ('885) paragraph 9).

5. As per claim 2, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said visual indicator is turned on when power is applied to said computer motherboard (Cowan ('128) column 1 lines 36-43, the yellow LED is lit when performing testing, and Dai ('885) paragraph 9, when BIOS are performing POST tests, these are done upon booting of the computer).

6. As per claim 3, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said visual indicator is turned off upon detection of a fault on said computer motherboard

(Cowan ('182) column 1 lines 36-40, when a test has failed, indicating a fault, the yellow light is disabled and the red LED is lighted).

7. As per claim 5, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said nonvolatile memory device stores power-on self-test diagnostic instructions and basic input and output system instructions (Dai ('885) paragraphs 7 and 9, and Cowan ('182) column 1 lines 26-28).

8. As per claim 6, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1 wherein said visual indicator is a light emitting diode (Cowan ('182) column 1 lines 35-43).

9. As per claim 7, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1 wherein said visual indicator is an external visual indicator (Cowan ('182) column 1 lines 23-25).

10. As per claim 9, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 7, further comprising an I/O port coupled to said microprocessor, said microprocessor providing signals to said external visual indicator via said I/O port (Cowan ('182) column 1 lines 13-19).

11. As per claim 10, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said computer motherboard includes integrated circuits mounted on said computer motherboard (Cowan ('182) Figure 5, the PC under test contains multiple components).

12. As per claim 11, this claim recites limitations found in claims 1-3. As claims 1-3 are disclosed by Cowan ('182) in view of Dai ('885), claim 11 is rejected over Cowan ('182) in view of Dai ('885) on the same reasoning as cited in claims 1-3.

13. As per claims 13-15, these claims recite limitations found in claims 5-7, respectively, and are rejected on the same grounds as claims 5-7.

14. As per claim 17, Cowan ('182) in view of Dai ('885) discloses the method for detecting and indicating faults on a computer motherboard as in claim 15, further comprising the step of initiating an I/O port coupled to said microprocessor, said microprocessor providing signals to said external visual indicator via said I/O port when said computer motherboard is not initialized successfully (Cowan ('182) column 1 lines 15-21 and 35-40, when a test fails the red LED is activated).

15. As per claim 18, this claim recites limitations found in claim 10 and is rejected on the same grounds as claim 10.

16. As per claim 19, Cowan ('182) discloses an apparatus for detecting and indicating faults in a computer motherboard comprising:

means for turning on a visual indicator (column 1 lines 36-40);

means for storing a plurality of diagnostic instructions (column 1 lines 27-31);

means for requesting and retrieving said plurality of diagnostic instructions (column 1 lines 27-31);

means for executing said retrieved plurality of diagnostic instructions (column 1 lines 27-31);

means for turning off said visual indicator when no fault is found on said computer motherboard (column 1 lines 36-40, the Yellow LED is deactivated upon the finishing of a test).

Testing by Cowan ('182) is performed within a TSR (column 4 lines 1-6). Cowan ('182) does not expressly disclose the apparatus comprising means for receiving an initialization signal to start a computer system; turning on a indicator when power is applied to said computer motherboard; retrieving diagnostic instructions upon reception of an initialization signal and instructions causing the initialization of said computer motherboard.

Dai ('885) discloses a BIOS test performed at power-on (paragraphs 7 and 9) that outputs test results to a series of LEDs (paragraph 14). BIOS performs initialization

routines for a motherboard (paragraph 9, BIOS are the first program run) wherein an initialization signal that starts the BIOS is a power up signal.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the testing performed by Cowan ('182) such that testing is performed on power up by the BIOS, as taught by Dai ('885), instead of within a TSR as disclosed by Cowan ('182). This modification would have been obvious because problems should be found before starting other (application) operations to ensure that the computer is running in the optimal mode (Dai ('885) paragraph 9).

17. As per claim 21, this claim recites limitations found in claim 7 and is rejected on the same grounds as claim 7.

18. As per claims 23, 24 and 25, these claims recite limitations from claims 5, 6 and 9, respectively, and are each rejected on the same grounds as respective claims 5, 6 and 9.

19. Claims 4, 12, 20 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowan ('182) in view of Dai ('885) and in further view of Model MK-70.

20. As per claim 4, Cowan ('182) in view of Dai ('885) discloses the apparatus for detecting faults on a motherboard as in claim 1. Cowen ('182) in view of Dai ('885) also discloses that the system checks for faults within the memory subsystem (Dai ('885) paragraph 7) and can activate an indicative LED upon the detection of a fault (Cowen ('182) column 1 lines 40-45).

Cowan ('182) in view of Dai ('885) does not explicitly disclose the apparatus further comprising a flash circuit activating a flash visual indicator upon detection of a fault.

Model MK-70 is an advertisement for flashing LED device.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the error notification system disclosed by Cowan ('182) in view of Dai ('885) such that it implements flashing LEDs for more serious errors. This would have been obvious because a flashing red light always gets attention (Model MK-70, right side, about the middle between the price per unit and the price for shipping and handling).

21. As per claim 12, Cowan ('182) in view of Dai ('885) discloses the method for detecting and indicating faults on a computer motherboard as in claim 11, further comprising the steps of:

initializing a memory subsystem (Cowan ('182) column 1 lines 30-32 and Dai ('885) paragraph 7, POST tests the memory); and

activating a visual indicator when a fault is found on said memory subsystem (Cowan ('182) column 1 lines 35-38).

Cowan ('182) in view of Dai ('885) does not explicitly disclose the method wherein the visual indicator is a flashing visual indicator.

Model MK-70 is an advertisement for flashing LED device.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the error notification system disclosed by Cowan ('182) in view of Dai ('885) such that it implements flashing LEDs for more serious errors. This would have been obvious because a flashing red light always gets attention (Model MK-70, right side, about the middle between the price per unit and the price for shipping and handling).

22. As per claim 20, this claim recites limitations found in claim 12 and is rejected on the same grounds as claim 12.

23. As per claim 26, Cowan ('182) discloses an apparatus for detecting and indicating faults on a computer motherboard comprising:

a host bus for transmitting address and data signals (as shown in Figure 5);

a nonvolatile memory device couple to said host bus having a plurality of diagnostic instructions stored (column 1 lines 26-29);

a microprocessor couple to said host bus, said microprocessor capable of request and retrieving said plurality of diagnostic and executing said retrieved plurality of diagnostic instructions (as shown in Figure 5 and column 1 lines 26-29);

a visual indicator coupled to said microprocessor (column 1 lines 15-23);

a general I/O port coupled to said microprocessor turning said visual indictor off when said computer mother board is not tested successfully (column 1 lines 35-40, the yellow LED is deactivated upon a failure); and

a circuit activating a visual indicator when a failure is found (column 1 lines 35-40, the red LED is activated upon a failure).

Testing by Cowan ('182) is performed within a TSR (column 4 lines 1-6). Cowan ('182) does not explicitly disclose the apparatus wherein the diagnostic instructions are POST and BIOS instructions, and are executed upon initialization and power up of the system and test a memory subsystem. Cowan ('182) additionally does not disclose the use of a flashing visual indicator when a test has failed.

Dai ('885) discloses a BIOS test performed at power-on (paragraphs 7 and 9) that outputs test results to a series of LEDs (paragraph 14). BIOS performs initialization routines for a motherboard (paragraph 9, BIOS are the first program run) wherein an initialization signal that starts the BIOS is a power up signal. The POST performed by BIOS also tests memory and other subsystems (paragraph 7).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the testing performed by Cowan ('182) such that testing is performed on power up by the BIOS, as taught by Dai ('885), instead of within a TSR as disclosed by Cowan ('182). This modification would have been obvious because problems should be found before starting other (application) operations to ensure that the computer is running in the optimal mode (Dai ('885) paragraph 9).

Model MK-70 is an advertisement for flashing LED device.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the error notification system disclosed by Cowan ('182) in view of Dai ('885) such that it implements flashing LEDs for more serious errors. This would have been obvious because a flashing red light always gets attention (Model MK-70, right side, about the middle between the price per unit and the price for shipping and handling).

24. As per claim 27, Cowan ('182) in view of Dai ('885) and Model MK-70 discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 26, wherein said external visual indicator is located on panel of said computer system (Cowan ('182) figure 1, element 20 is the connector (also see column 1 lines 17-22) containing the LEDs and connecting wires to the system under test).

25. As per claim 28, Cowan ('182) in view of Dai ('885) and Model MK-70 discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 26, wherein said computer motherboard comprises integrated circuit mounted on said computer motherboard (Cowan ('182) Figure 5, the PC under test contains multiple components).

26. Claims 8, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cowan ('182) in view of Dai ('885) and in further view of BOXX Box Boxes Clever.

27. As per claim 8, Cowan ('182) in view of Dai ('885) disclose the apparatus for detecting and indicating faults in a computer motherboard as in claim 1. Cowan ('182) in view of Dai ('885) does not explicitly disclose the apparatus wherein said visual indicator is an internal visual indicator.

BOXX Box Boxes Clever is a review of a computer casing.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Cowan ('182) in view of Dai ('885) such that when they are unneeded, the diagnostic LEDs can be concealed. This modification would have been obvious because bright LEDs can be so annoying to a casual computer user that he may attempt to manually conceal them (BOXX Box Boxes Clever, third paragraph from the end).

28. As per claims 16 and 22, these claims recite the same limitations as claim 8 and are rejected on the same grounds as claim 8.

### *Conclusion*

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Chen ('707) teaches a system wherein LEDs convey the functionality of the motherboard during operation, Grants ('883) and Matsumoto ('922) teach systems that uses a LED to indicate which component of a system experienced a fault, and Park ('157) teaches a system that uses multiple LEDs to indicate which state of a POST process is being executed.

### *Contact Information*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER